WHAT IS CLAIMED IS:

1. A method for protecting integrated circuitry from induced charge damage during device fabrication, the method comprising:

forming an ONO layer on a substrate, the ONO layer having an opening therein;

filling the opening with a thin insulating layer; and

forming a polysilicon layer on the ONO layer and the thin insulating layer.

2. The method of claim 1 wherein filling the opening with a thin insulating layer comprises providing an oxide layer with a thickness of no more than about eighty Angstroms.

3. The method of claim 2 further wherein the thicknesss of the thin oxide layer is less than about 60Å.

4. The method of claim 1 further comprising creating an n-well in the substrate prior to forming the ONO layer, where the opening in the ONO layer is over the n-well.

5. The method of claim 4 further comprising forming an n+well at a junction between the substrate and the n-well.

6. The method of claim 4 further comprising creating a p-well within the n-well, wherein the opening in the ONO layer is over the p-well.

7. The method of claim 6 further comprising forming a p+well adjacent the p-well.

8. The method of claim 1 further comprising isolating the thin oxide layer from the substrate with a PN junction.

9. The method of claim 1 further comprising isolating the thin oxide layer from the substrate by a pair of back-to-back PN junctions.

10. The method of claim 9 wherein the PN junctions function as diodes.

11. A structure for protecting NROM devices from charge induced damage during device fabrication, the structure comprising:a substrate;

an ONO layer disposed on the substrate, the ONO layer having an opening therein;

a thin insulative layer disposed on the substrate within the opening in the ONO layer; and

a polysilicon layer disposed on the ONO layer and on the thin insulative layer the polysilicon layer being coupled to circuitry to be protected.

12. The structure of claim 11 wherein the thin insulative layer comprises a thin oxide layer.

13. The structure of claim 12 wherein the thin oxide layer has a thickness less than about 80Å.

14. The structure of claim 13 wherein the thin oxide layer has a thickness less than about 60Å.

15. The structure of claim 12 further comprising a first PN junction between the thin oxide layer and the substrate.

16. The structure of claim 15 wherein the first PN junction comprises an n-well in a p-type substrate.

17. The structure of claim 16 further comprising a second PN junction.

18. The structure of claim 17 wherein the second PN junction comprises a p-well within the n-well.

19. The structure of claim 18 further comprising an n+well at a junction between the n-well and the substrate.

20. The structure of claim-19 further comprising a p+well adjacent to the p-well.